Docket:
90065.146801/17732.6317.003

MOS-GATED DEVICE HAVING A BURIED GATE AND PROCESS FOR FORMING SAME

Cross-Reference to Related Applications

This application is a divisional application of U.S. Patent Application Serial No. 09/260,411, filed March 1, 1999 (Attorney Docket No. 90065.99R022), now U.S. Pat. No. 6351009.

Field of the Invention

The present invention relates to semiconductor devices and, more particularly, to an MOS-gated device and a process for forming same.

Background of the Invention

An MOS transistor that includes a trench gate structure offers important advantages over a planar transistor for high current, low voltage switching applications. In the latter configuration, constriction occurs at high current flows, an effect that places substantial constraints on the design of a transistor intended for operation under such conditions.

A trench gate of a DMOS device typically includes a trench extending from the source to the drain and having sidewalls and a floor that are each lined with a layer of thermally grown silicon dioxide. The lined trench is filled with doped polysilicon. The structure of the trench gate allows less constricted current flow and, consequently, provides lower values of specific on-resistance. Furthermore, the trench gate makes possible a decreased cell pitch in an MOS channel extending along the vertical sidewalls of the trench from the bottom of the source across the body of the transistor to the drain below. Channel density is thereby increased, which reduces the contribution of the channel to on-resistance. The structure and performance of trench DMOS transistors are discussed in Bulucea and Rossen, "Trench DMOS Transistor Technology for High-Current (100 A Range) Switching," in Solid-State Electronics, 1991, Vol. 34, No. 5, pp 493-507, the disclosure of which is incorporated herein by reference. In addition to their utility in DMOS devices, trench gates are also advantageously employed in insulated gate bipolar transistors (IGBTs), MOS-controlled

thyristors (MCTs), and other MOS-gated devices.

FIG. 1 schematically depicts the cross-section of a trench MOS gate device 100 of the prior art. Although FIG. 1 shows only one MOSFET, a typical device currently employed in the industry consists of an array of MOSFETs arranged in various cellular or stripe layouts.

Device 100 includes a doped (depicted as N+) substrate 101 on which is grown a doped epitaxial layer 102. Epitaxial layer 102 includes drain region 103, heavily doped (P+) body regions 104, and P-wells 105. Abutting body regions in epitaxial layer 103 are heavily doped (N+) source regions 106, which are separated from each other by a gate trench107 that has dielectric sidewalls 108 and floor 109. Gate trench 107 is substantially filled with gate semiconductor material 110. Because the source regions 106 and gate semiconductor material 110 have to be electrically isolated for device 100 to function, they are covered by a dielectric layer 111. Contact openings 112 enable metal 113 to contact body regions 104 and source regions 106.

Contact openings 112 are formed in dielectric layer 111, which typically is a deposited layer of oxide, by conventional mask/etch techniques. The size of device 100 depends on the minimum thickness of dielectric needed for isolation (the lateral distance between a source region 106 and gate trench 107) and on the tolerance capabilities of the mask/etch procedures. The thickness of dielectric layer 111 is determined not only by the minimum required voltage isolation but also on the need to minimize source-to-gate capacitance, which affects device switching speed and switching losses. Switching losses are directly proportional to the capacitance, which is in turn inversely proportional to the dielectric thickness. Therefore there is a typical minimum thickness of about 0.5-0.8 μm for dielectric layer 111 in prior art device 100.

As just noted, the required minimum thickness of dielectric layer 111 imposes limitations on the minimum size of device 100. It would be desirable to be able to reduce the size and improve the efficiency of semiconductor devices. The present invention provides these benefits.

Summary of the Invention

The present invention is directed to an improved trench MOS-gated device formed on a monocrystalline semiconductor substrate comprising a doped upper layer. The doped upper

layer, includes at an upper surface a plurality of heavily doped body regions having a first polarity and overlying a well region and a drain region. The upper layer further includes at its upper surface a plurality of heavily doped source regions that have a second polarity opposite that of the body regions and extend to a selected depth in the upper layer.

A gate trench extends from the upper surface of the upper layer through the well region to the drain region and separates one source region from a second source region. The trench has a floor and sidewalls comprising a layer of dielectric material and contains a conductive gate material filling the trench to a selected level and an isolation layer of dielectric material that overlies the gate material and substantially fills the trench. The upper surface of the overlying layer of dielectric material in the trench is thus substantially coplanar with the upper surface of the upper layer.

Also in accordance with the present invention is a process for forming an improved, high density, self-aligned trench MOS-gated device. A doped upper layer having an upper surface and an underlying drain region is formed on a substrate, and a well region having a first polarity is formed in the upper layer over the drain region. A gate trench mask is formed on the upper surface of the upper layer, and a plurality of gate trenches extending from the upper surface through the well region to the drain region are etched in the upper layer.

Sidewalls and a floor each comprising a dielectric material are formed in each of the gate trenches, which are filled to a selected level with a conductive gate material. The trench mask is removed, and an isolation layer of dielectric material is formed on the top surface of the upper layer and within the gate trench, where it overlies the gate material and substantially fills the trench. The dielectric layer is removed from the top surface of the upper layer; the dielectric layer remaining within the trench has an upper surface that is substantially coplanar with the upper surface of the upper layer.

A plurality of heavily doped body regions having a first polarity are formed at the upper surface of the upper layer. A source mask is formed on the upper surface, and a plurality of heavily doped source regions having a second polarity and extending to a selected depth into the upper layer are formed in the body regions. Following removal of the source mask, a metal contact to said body and source regions is formed over the upper surface of the upper layer.

Brief Description of the Drawings

FIG. 1 schematically depicts a cross-section of a trench MOS-gated device 100 of the prior art.

FIG. 2 is a schematic cross-sectional representation of a trench MOS-gated device 200 of the present invention; FIGS. 2A-D illustrate the process of forming device 200.

FIGS. 3A and 3B schematically depict cross-sections of another device 300 in accordance with the present invention; FIG. 3C is a schematic plan view of device 300.

Detailed Description of the Invention

The trench MOS-gated device of the present invention, by eliminating the surface area required for gate-source dielectric isolation, enables the size of the device to be substantially reduced. A masking procedure to form contact openings in the dielectric layer is also avoided; the gate trench of the invention is thus self-aligned.

FIG. 2 depicts an improved trench MOS-gated device 200 of the present invention. Device 200 includes a doped N+ substrate 201 on which is deposited an epitaxial doped upper layer 202. Epitaxial layer 202 includes drain region 203, heavily doped P+ body regions 204, and P-well regions 205. Abutting body regions 204 in epitaxial layer 203 are heavily doped N+ source regions 206, which are separated from each other by a gate trench 207 that has dielectric sidewalls 208 and floor 209. Contained within trench 207 is a gate material 210, filled to a selected level 211, and an overlying dielectric layer 212. Selected level 211 of gate material 210 is approximately coplanar with the selected depth 216 of N+ source regions 206, thereby providing overlap between source regions 206 and gate material 210. The surface 213 of gate dielectric layer 212 is substantially coplanar with the surface 214 of epitaxial layer 202. Deposited metal layer 215 is able to contact body regions 204 and source regions 206 without the need for a masking procedure to form contact openings, as was required for prior art device 100.

Because gate material 210 is recessed within gate trench 207 to permit the inclusion of dielectric layer 212 of sufficient thickness to provide gate isolation, diffusions to form N+

source regions 206 must be deep enough to ensure overlap with gate material 210. Although source regions 206 are shown as having N polarity and body regions 204 are depicted as having P polarity in device 200, it is understood that the polarities of these regions can be reversed from those shown in FIG. 2.

FIGS. 2A-D schematically illustrate the process of forming device 200. As shown in FIG. 2A, on a doped semiconductor substrate 201, which can be monocrystalline silicon, is formed a doped upper layer 202 that includes a drain region 203. Upper layer 202 can be epitaxially grown silicon or, for lower voltage devices (ca 12V), a heavily doped portion of substrate 201. P well regions 205 are formed in layer 202 by doping into upper layer surface 214. A trench mask TM patterned to define a gate trench is formed on surface 214, and gate trench 207 extending through P-well regions 205 to drain region 203 is etched in layer 202. Trench dielectric sidewalls 208 and floor 209, preferably comprising silicon dioxide, which can be either deposited or grown, are formed in gate trench 207, which is then filled with a conductive gate material 210, which can be, for example, a metal, a silicide, or doped polysilicon, to a selected depth 211.

Referring to FIG. 2B, following removal of trench mask TM, filling of trench 207 is completed by forming an isolation dielectric layer 212, which can be silicon dioxide, over gate material 210 in trench 20 and on surface 214. A planarization dielectric etch is performed to re-expose surface 214 without removing dielectric material 212 from trench 207. Surface 213 of dielectric layer 212 in trench 207 is thereby rendered substantially coplanar with upper surface 214 of layer 202. It may be advantageous, however, to etch surface 213 slightly below surface 214 in order to increase source contact and improve device on-resistance characteristics.

Also as shown in FIG. 2B, N+ source regions 206 are formed in layer 202 by ion implantation and diffusion to a selected depth 216 that is approximately coplanar with selected level 211 of dielectric material 210 and thereby provides overlap between gate material 210 and source regions 206.

Referring to FIG. 2C, a body mask M is formed on surface 214, and P+ body regions 204 are formed by further doping of layer 202. Removal of the body mask M, followed by deposition of metal 215 to provide contact with body regions 204 and source regions 206, completes the formation of device 200, as shown in FIG. 2D. Metal (not shown) can be

deposited on the reverse side of the substrate to provide contact with drain region 203. Although in the just described fabrication sequence, the formation of source regions 206 preceded the formation of body regions 204, it is recognized that this ordering is not critical and that the described masking procedure can be varied for the purpose of convenience.

Gate trenches 207 included in a device of the present invention may have an open-cell stripe topology or a closed-cell cellular topology. Furthermore, in the closed- cell cellular topology, the trenches may have a square or, more preferably, a hexagonal configuration. Although device 200, as schematically depicted in FIG. 2, is a power MOSFET, the present invention is applicable to the construction of other MOS-gated devices such as an insulated gate bipolar transistor (IGBT), an MOS-controlled thyristor (MCT), and an accumulation field effect transistor (ACCUFET).

FIGS. 3A-C depict an alternative embodiment of the present invention. Device 300 includes a doped N+ substrate 301, on which is disposed a doped upper layer 302. Upper layer 302 includes drain region 303 and P-wells 305. As shown in FIG. 3A, P+ body regions 304 are formed in layer 302 and separated from each other by a gate trench 307. Similarly, as depicted in FIG. 3B, N+ source regions 306, formed by ion implantation and diffusion to a selected depth 316 in upper layer 302, are also separated by gate trench 307. Gate trenches 307 each have dielectric sidewalls 308 and a floor 309 and contain conductive gate material 310, filled to a selected level 311, and an overlying dielectric layer 312. The surface 313 of gate dielectric layer 312 is substantially coplanar with the surface 314 of upper layer 302. Metal layer 315 is deposited on surface 314 to contact body regions 304 and source regions 306.

As shown in FIG. 3C, device 300 includes a plurality of arrays 317 of alternating P+ body regions 304 and N+ source regions 306. Each array 317 is disposed adjacent to a gate trench 307 and separated from a second array 317 by the gate trench 307. Also, as depicted in FIG. 3C, source regions 306 comprise a greater portion, body regions 304 a lesser portion, of the lengthwise dimension of an array 317 disposed alongside a gate trench 307.

In the formation of device 300, following the planarization of dielectric layer 312 to re-expose surface 314, P+ body regions are formed in upper layer 302 by doping. A non-critical source mask (not shown), disposed transversely to trenches 307, is formed on surface 314, and source regions 306 are formed by ion implantation and diffusion. The arrangement

of body regions 304 and source regions 306 in arrays 317 separated by gate trenches 307, as depicted for device 300 in FIGS. 3A-C, further exploits the advantage of device size reduction provided by present invention.

The invention has been described in detail for the purpose of illustration, but it is understood that such detail is solely for that purpose, and variations can be made therein by those skilled in the art without departing from the spirit and scope of the invention, which is defined by the following claims.